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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,497	03/25/2004	Sung-ho Kim	SEC.1147	5716

20987 7590 01/24/2006

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EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,497	KIM ET AL.	
	Examiner	Art Unit	
	Thinh T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Applicant's election of claims 1-14 for prosecution without traverse in the communication with the Office on 11/09/2005 is acknowledged.

Specification

2. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Drawings

3. Fig. 1 is not designated by a legend such as " prior art ". The legend is necessary in order to clarify what applicant 's invention is (see MPEP paragraph 608.02).

4. The Drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the drawing showing a nonvolatile semiconductor memory device wherein the junction region and a channel region of the byte select transistor are disposed in an undoped native semiconductor substrate (in claim 5) wherein the junction region and a channel region of the byte select transistor are disposed in a doped conductive well region (in claim 6) . wherein

the junction region and a channel region of each of the 1-byte memory transistors are disposed in the doped conductive well region. (in claim 7) must be shown or the features cancelled from the claims. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in the reply to the Office Action to avoid abandonment of the Application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(a/b/e) that form the basis for the rejections under this section made in this office action.

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3,11 are rejected under 35 U.S.C. 102(b) as being anticipated by Cappelletti et al. (U.S. Patent 5,612,913).

REGARDING CLAIM 1

Cappelletti 913 (in the Abstract, in fig 1, fig 3, fig 4) discloses a nonvolatile semiconductor memory device comprising: a semiconductor substrate comprising an active region and an isolation region; 1-byte memory transistors arranged in a first

direction, wherein each of the 1-byte memory transistors includes a junction region and a channel region formed in the active region of the semiconductor substrate; and a byte select transistor disposed in the active region, wherein the byte select transistor includes a junction region that is directly adjacent to the junction of each of the 1-byte memory transistors. (noted that the source selected gate is the byte selected transistor since in fig 3 the drain of the source select transistor in Cappelletti 913 reference is connected to the segment of 8 drains of 8 transistors of the byte memory cells).

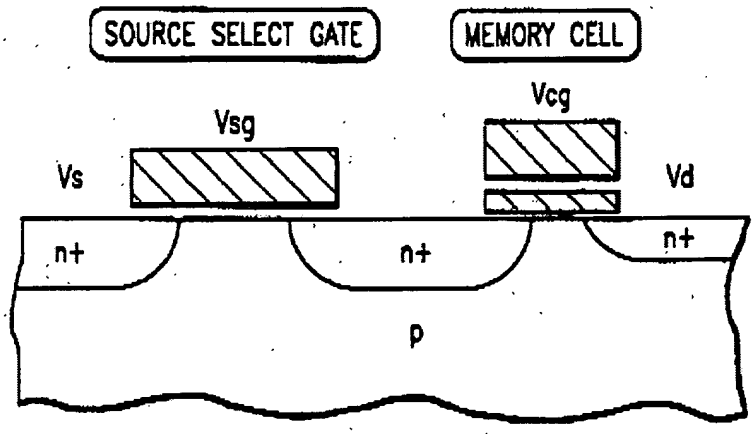
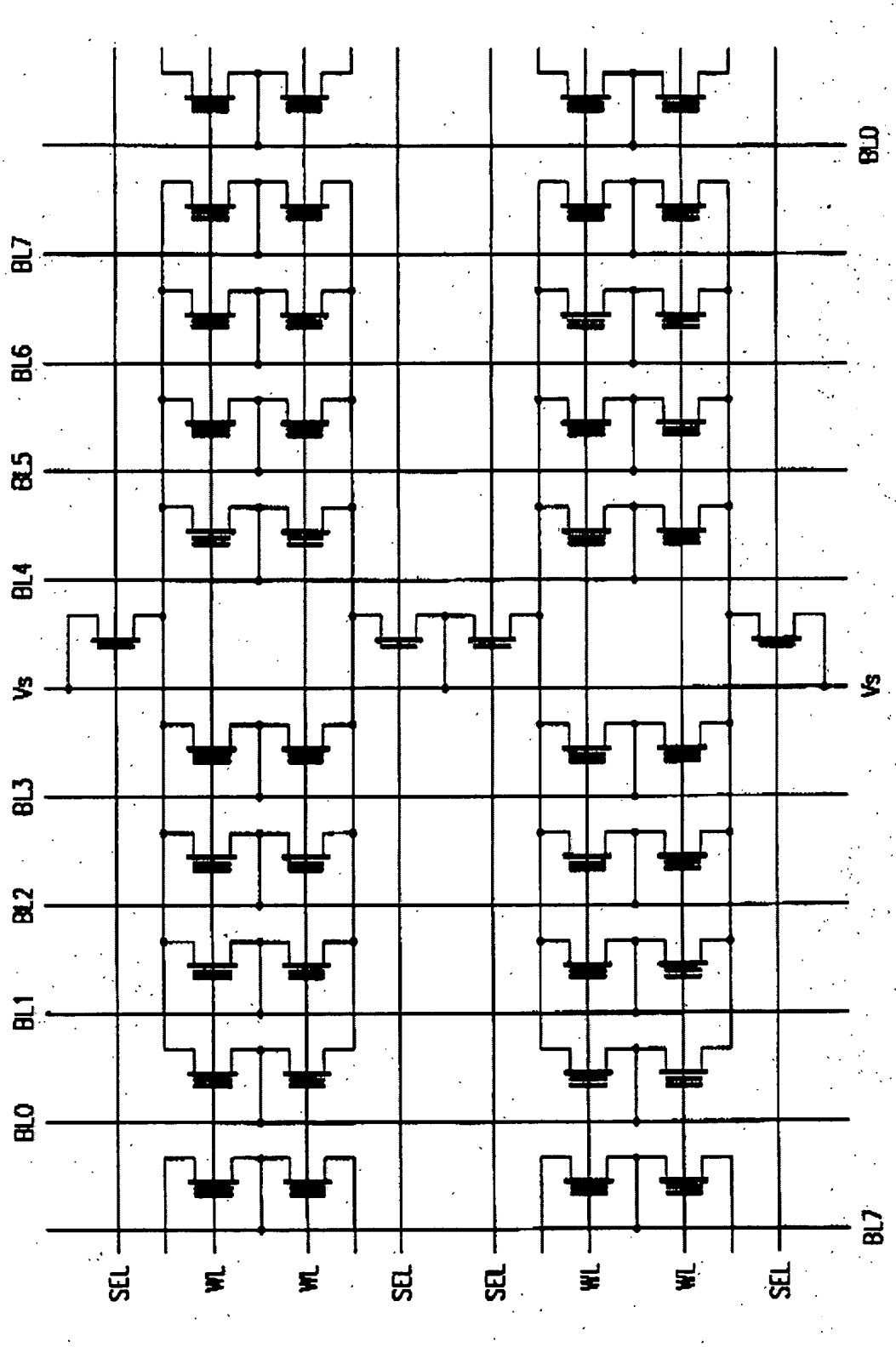


FIG. 4

FIG. 3


BL0
BL7
BL6
BL5
BL4
Vs
BL3
BL2
BL1
BL0
SEL
WL
WL
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WL
WL
SEL
BL0
Vs
BL7

REGARDING CLAIM 2

Cappelletti 913 (in the Abstract, in fig 3, fig 4) discloses a non-volatile semiconductor memory wherein the byte select transistor is disposed over or under the 1-byte memory transistors perpendicular to the arranged direction of the 1-byte memory transistors.

REGARDING CLAIM 3

Cappelletti 913 (in the Abstract, in fig 3, fig 4) discloses a non-volatile semiconductor memory wherein the junction of each of the 1-byte memory transistors that is directly adjacent to the junction of the byte select transistor is a source region.

REGARDING CLAIM 5

Cappelletti 913 (in the Abstract, in fig 4) discloses a non-volatile semiconductor memory wherein the junction region and a channel region of the byte select transistor are disposed in an undoped native semiconductor substrate.

REGARDING CLAIM 11

Cappelletti 913 (in the Abstract, in fig 3, fig 4) discloses a non-volatile semiconductor memory wherein each of the 1-byte memory transistors is a floating-gate-type transistor

Claim Rejections - 35 USC § 103

7. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 ,9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (U.S. Patent 5,612,913) in view of further remark.

REGARDING CLAIM 4

Cappelletti 913 discloses all the invention except for the features that the byte selected transistor is adjacent to the to the junction of each of the 1-byte transistors is the drain region.

This feature, however, is considered obvious since the applicant has not disclosed the switching from source to drain of the 1-byte transistor solve any stated problem or is for any particular purpose and it appear that The Invention by Cappelletti would perform equally well when the byte selected transistor is adjacent to the to the junction of each of the 1-byte transistors is the drain region. Also noted that the non-volatile 1- byte memory cells in the Cappelletti reference is symmetrical.

REGARDING CLAIM 9-10

Cappelletti discloses all the invention except for the channel relative width of the byte select transistor compare with the byte-cell transistors and the width of the isolation. These features, however, are considered obvious since it has been held that where the general condition of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art.

A person skilled in the art at the time the invention was made would have been fully capable of using the teachings by Cappelletti and routine experimentation in the lab or software optimization and simulation tool and come up with the invention of claims 9-10 without any special instruction.

9. Claim 6,7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (U.S. Patent 5,612,913). in view of Caywood (US patent Application Publication 2002/0191439)

REGARDING CLAIM 6,7

Cappelletti discloses all the invention of claim 6,7 except is silent about the limitations that required that the junction region and a channel region of the byte select transistor are disposed in a doped conductive well region and a channel region of each of the 1-byte memory transistors are disposed in the doped conductive well region. Caywood, however, discloses in paragraph [0119] that the junction region and a channel region of the byte select transistor are disposed in a doped conductive well region and a channel region of each of the 1-byte memory transistors are disposed in the doped conductive well region

It would have been obvious to one of ordinary skill in the art the time the invention was made to complement the teachings by Cappelletti with the teachings by Caywood, and come up with the invention of claims 6,7

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to improve the device invented by Cappelletti using the teachings by Caywood, and come up with a superior device that can work with a lower operating voltage as taught by Caywood in his abstract.

10. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (U.S. Patent 5,612,913) in view of Blyth et al. (US patent 6,400,603).

REGARDING CLAIM 8

Cappelletti discloses all the invention except for the use of the source side injection byte memory cells; Blyth, however, discloses a flash memory (the abstract) that uses source side injection byte memory cells;

It would have been obvious to one of ordinary skill in the art the time the invention was made to complement the teachings by Cappelletti with the teachings by Blyth and come up with the invention of claims 8

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to improve the device invented by Cappelletti using the teachings by Blyth and come up with a superior device that use less programming current as disclosed in Blyth reference (column 12 line 30-36).

11. Claims 12, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (U.S. Patent 5,612,913) in view of Wu et al. (US patent 6,445,030).

REGARDING CLAIM 12

Cappelletti discloses all the invention except for the use of memory cell structure using silicon-oxide-nitride-oxide-silicon-type transistor ; Wu, however, (in the abstract, in fig 7) discloses a flash memory cell having silicon-oxide-nitride-oxide-silicon-type transistor. It would have been obvious to one of ordinary skill in the art the time the invention was made to complement the teachings by Cappelletti with the teachings by Wu and come up with the invention of claims 12

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to improve the device invented by Cappelletti using the teachings by Wu in order to come up with a device that has improved erase speed as suggested by Wu in the abstract .

REGARDING CLAIM 13

Wu discloses a non-volatile memory device, (in the abstract, in fig 7) wherein a gate electrode structure of the silicon-oxide-nitride-oxide-silicon-type transistor type includes a first oxide layer, a nitride layer, a second oxide layer, and a conductive layer, which are sequentially stacked and have substantially the same width. The rationale as why claim 13 is obvious over Cappelletti in view of Wu has been set forth in the rejection of claim 12 above.

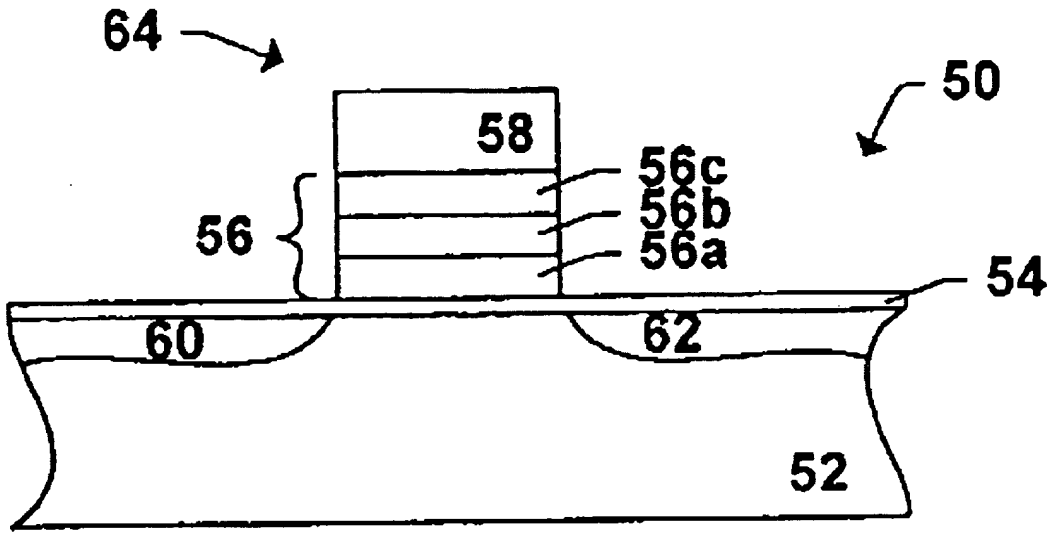


FIG. 7

Wu et al. reference

12. Claims 12, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (U.S. Patent 5,612,913) in view of Kang et al. (US patent 6,794,711)

The applied reference By Kang (US patent 6,794,711) has a common Assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of

this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

REGARDING CLAIM 12

Cappelletti discloses all the invention except for the use of memory cell structure using silicon-oxide-nitride-oxide-silicon-type transistor ; Kang however, (in the abstract, in fig 7A) discloses a non-volatile memory cell having silicon-oxide-nitride-oxide-silicon-type transistor.

It would have been obvious to one of ordinary skill in the art the time the invention was made to complement the teachings by Cappelletti with the teachings by Kang and come up with the invention of claims 12.

The rationale is as the following:

A person skilled in the art at the time the invention was made would have been motivated to improve the device invented by Cappelletti using the teachings by Kang in

order to come up with a device that can control the current in the channel region as suggested by Kang in the summary of the invention (column 2 lines 38-45) .

REGARDING CLAIM 14

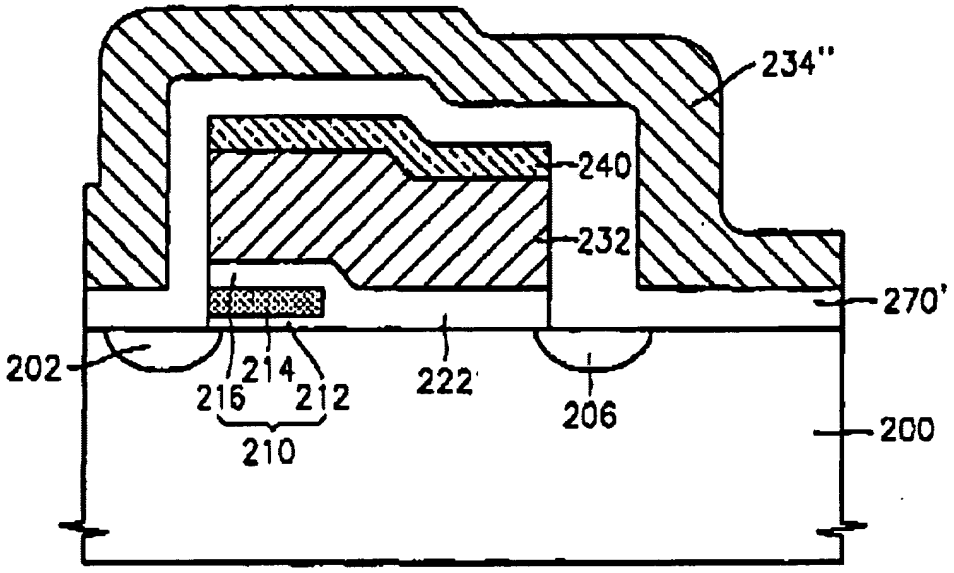
Cappelletti discloses all the invention except for the use of memory cell structure using silicon-oxide-nitride-oxide-silicon-type transistor ;wherein: a gate electrode structure of the silicon-oxide-nitride-oxide-silicon-type transistor or the metal-oxide-nitride-oxide-silicon-type transistor includes a first oxide layer, a nitride layer, a second oxide layer, and a conductive layer stacked sequentially; the first oxide layer, the second oxide layer, and the conductive layer have substantially the same width; and the nitride layer has a width smaller than the first oxide layer, the second oxide layer, and the conductive layer.

Kang however, (in the abstract, in fig 7A) discloses a non-volatile memory cell having silicon-oxide-nitride-oxide-silicon-type transistor.

wherein: a gate electrode structure of the silicon-oxide-nitride-oxide-silicon-type transistor or the metal-oxide-nitride-oxide-silicon-type transistor includes a first oxide layer, a nitride layer, a second oxide layer, and a conductive layer stacked sequentially; the first oxide layer, the second oxide layer, and the conductive layer have substantially the same width; and the nitride layer has a width smaller than the first oxide layer, the second oxide layer, and the conductive layer.

The rationale as why claim 14 is obvious over Cappelletti in view of Kang has been set forth above.

FIG. 7B



KANG reference

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

14. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

15. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d) which papers have been placed of record in the file.

CONCLUSION

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:30am-6: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thinh T. Nguyen

Art Unit 2818

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Supervisory Patent Examiner
Technology Center 2800